Amendments to the Specification:

Replace the Abstract at page 21 with the following new Abstract:

--Phase-locked loop (PLL) circuits include first and second PLL stages and use fractional frequency division. In one implementation, the first stage includes a voltage-controlled oscillator (VCO) whose output is provided to both first and second fractional frequency dividers. The output of the first frequency divider is provided to a first phase comparator whose output passes through a filter so as to provide the deviation signal that controls the output frequency of the first VCO. The output of the second fractional frequency divider is received by the second PLL stage as a reference signal. --